NRL Report 8334

Broadband GaAs MESFET Power Amplifier Design Aspects

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Final rept.

October 12, 1979

F34372

NAVAL RESEARCH LABORATORY
Washington, D.C.

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER NRL Report 8334	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) BROADBAND GaAs MESFET POWER AMPLIFIER DESIGN ASPECTS		5. TYPE OF REPORT & PERIOD COVERED Final report on one phase of a continuing NRL problem
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) H. A. Willing and W. H. Ku*		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Research Laboratory Washington, D.C. 20375		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS NRL Problem 52R08-87 Program Element 62734N Project No. ZF34-372
11. CONTROLLING OFFICE NAME AND ADDRESS CND Direct Funded Programs Naval Research Laboratory Washington, D.C. 20375		12. REPORT DATE October 12, 1979
		13. NUMBER OF PAGES 49
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

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Department, Cornell University, Ithaca, NY 14853.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Wideband
GaAs MESFET
Power amplifier

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report presents design aspects of ultra-wideband GaAs MESFET power amplifiers which are directed to ECM and EW system applications. Fundamental gain-bandwidth limitations are derived for state-of-the-art GaAs MESFET power devices. Broadband designs are developed in the 2- to 18-GHz range using analytical and computer-aided optimization techniques. These designs are based upon small- and large-signal device characterization and modeling. Presented are systematic procedures required to arrive at the final designs. Modeling techniques and their utilization as a tool in achieving optimum performance are described. Included in this report is a discussion of the laboratory methods employed to perform small- and large-signal device characterization and analysis.

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BROADBAND GaAs MESFET POWER AMPLIFIER DESIGN ASPECTS

1. INTRODUCTION

Recent advances in the development of GaAs MESFET devices have resulted in the achievement of impressive power-gain performance levels well into the microwave region. Power levels of 1 W and greater with gains of 5 dB have been reported at Ku-band frequencies [1,2]. These results were obtained at single frequencies or within very narrow frequency bands where the device was tuned for optimum performance. The devices were state-of-the-art or laboratory types which had not reached production status. They were structured in single- and multiple-cell configurations with increasing gate widths to obtain greater output power levels. With increasing cell size, the difficulty of achieving optimum wideband performance increases. Broadband power amplifier design requires extensive large- and small-signal characterization and analysis of device-circuit interactions to permit synthesis of matching networks.

This report describes the techniques required to successfully implement the optimum design of broadband GaAs power MESFET amplifiers. Small- and large-signal characterization techniques are discussed and circuit-type models which simulate device performance are described. These models include unilateral lumped and distributed equivalent circuit-type models for use in the synthesis of broadband matching networks. The development of single-ended amplifiers for operation in the 6- to 18-GHz range is also reported. These amplifiers were designed using existing small-signal device characterization and modeling techniques. At the start of this program, large-signal device models for design applications were not complete. However, a discussion of recent developments in large-signal modeling and their implementation for improved power amplifier designs is presented. The amplifiers discussed employ single- and dual-cell devices of 0.8-μm gate length (ℓ_g) and 300-μm gate width (ℓ_w) cell sizes. Performance characteristics of these amplifiers are given.

Further discussions of broadband power amplifier design aspects are presented in Appendices A and B. Projected performance of octave and multioctave amplifiers in the 2- to 18-GHz range are also included.

2. TECHNIQUES FOR DEVICE CHARACTERIZATION AND PERFORMANCE ANALYSIS

Achievements in the development of GaAs power MESFET devices are rapidly advancing. Devices with modified doping profiles, lower thermal resistances, reduced parasitics, and higher breakdown voltages are being developed for improved power-gain performance [3-7]. To permit trade-off analyses on output power and gain performance, extensive laboratory measurements of those devices are required. In this section performance characteristics of selected state-of-the-art GaAs power MESFET devices are

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presented. The devices were developed by Texas Instruments, Inc. in single-cell sizes of 300-μm gate width (ℓ_w) and 1-μm and 0.8-μm gate lengths (ℓ_g) with uniform doping profiles. Single-ended amplifiers employing the 300- $\times$ 0.8-μm device in single- and dual-cell configurations were designed, fabricated, and tested, and this work is reported in Sections 3 and 4.

Performance factors governing device characterization requirements for power amplifier designs are predominantly linearity, power gain, and efficiency. Designs based upon measured device S-parameters can achieve optimum small-signal gain performance. However, optimum power gain and/or efficiency performance levels may not be attained and require the implementation of large-signal device characterization techniques. An analysis of the influence of these factors on GaAs power MESFET amplifier designs follows.

Laboratory Measurement Methods

Extensive small- or large-signal device characterization is required to achieve optimum wideband power amplifier performance. Laboratory measurement methods used to obtain this information include the employment of a network analyzer yielding small-signal S-parameters, and "load-pulling" techniques to obtain large-signal device characterization. Fundamental to the small-signal device characterization is the requirement to de-embed the device from the test network. A technique was developed by R.E. Neidert of the Naval Research Laboratory to correct for test fixture modifications to measured device S-parameters. This technique is fully described in NRL Memorandum Report 4015 [8]. In its simplest form, the test fixture is comprised of symmetric, low-VSWR, input and output circuits. The test fixture used to obtain the device S-parameters given in this report is shown in Fig. 1. Device S-parameters are determined by dividing measured S-parameters of the device plus test fixture by the measured-through S_{21}-parameters of the test fixture (Fig. 1) only at the associated frequencies.
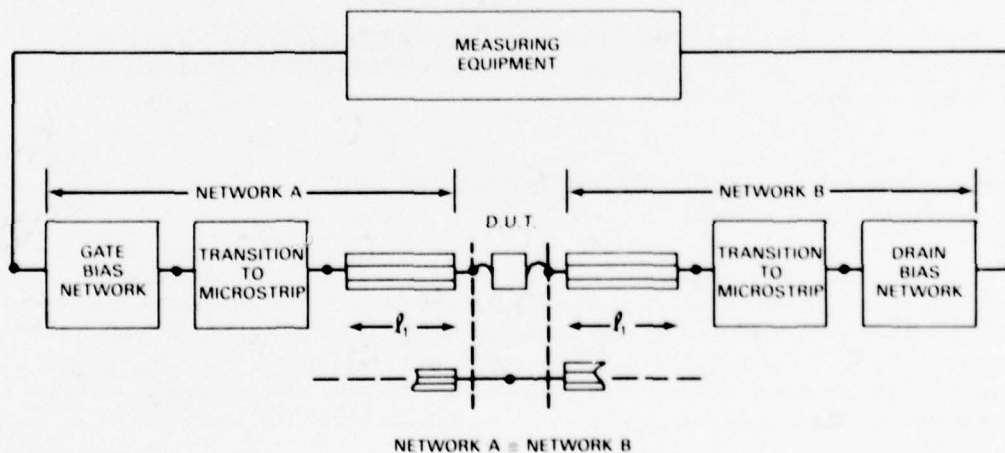

Fig. 1 — Test fixture for Device Under Test (D.U.T.).

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Large-signal device characterization via load-pulling can be implemented through manual or mechanical means. Manual methods require tuning of input and output networks in conjunction with the device under test to establish monitored performance levels. Tuning is performed at selected frequencies within the desired range of operation. The networks tuned to each frequency are separated from the device; and subsequently the input and output impedance levels presented to the device are experimentally determined. The negative aspects of this technique are its time-consuming nature and the difficulty of fully assessing circuit losses occurring when matching between high-impedance ratios. The technique however can be mechanically implemented and automated to greatly reduce the amount of testing time [9]. An equivalent method which simulates complex load conditions is described by Takayama [10]. This approach simplifies the measurement requirements. A circuit description of this technique is given in Fig. 2. As illustrated, a portion of the input signal to the device under test is used to simulate the reflected signal of an arbitrary output load. The amplitude and phase of this signal is adjusted to provide the desired complex load impedance conditions at the drain port of the device. Direct measurements of the simulated load impedance are made with a reflection test unit. This technique permits in-situ device characterization and negates the circuit loss problems associated with direct circuit-tuning methods.

Device Models

An alternative to full device characterization and performance analysis by laboratory measurements is device modeling. Accurate circuit-type models have been described which simulate small-signal device performance [11,12]. In addition, analytical [13,14] and numerical [15,16] models are being developed. They provide a fuller understanding of the influence of material and physical parameters on device performance.

The circuit-type model shown in Fig. 3 can be used to accurately simulate device S-parameters into the Ku-band region. For a given bias condition the parameter value of each model element can be determined by least-square-fitting the model-predicted, frequency-dependent S-parameters to measured S-parameters. The small-signal model element values can be derived by fitting to measurements outside the frequency band of design. However, the model may then be used to predict the S-parameters within the design band. This provides the flexibility of choosing differing frequency ranges of measurement and design.

A quasi-static or large-signal device model was developed at the Naval Research Laboratory [17,18]. This model provides a technique for simulating nonlinear performance of a GaAs MESFET interfacing with arbitrary complex load conditions. The technique is based on the circuit-type model used to describe small-signal performance. The quasi-static model consists of linear and nonlinear elements as identified in Fig. 3. Instantaneous values of each nonlinear element are given by relationships expressed in the form of instantaneous voltages. These voltage-dependent relationships were derived from bias-dependent values of the small-signal (incremental) model elements determined from measured sets of S-parameters. The sets were taken for discrete combinations of drain-to-source voltage V_{DS} and gate-to-source voltage V_{GS}.

A quasi-static model, developed to describe the performance characteristics of a 600-μm (ℓ_w) × 1.7-μm (ℓ_g) GaAs FET, was used to demonstrate the value of this technique

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Fig. 2 — A load-pulling test system

PACKAGE PARASITIC ELEMENTS:
L_S, L_G, L_D, C_P

FIXED DEVICE ELEMENTS:
C_G, C_{EX}, C_{GD}, R_G, R_D, R_S, C_O

NONLINEAR DEVICE ELEMENTS:
C_{FB}, C_{IN}, G_M, R_{IN}, R_{GD}, R_O
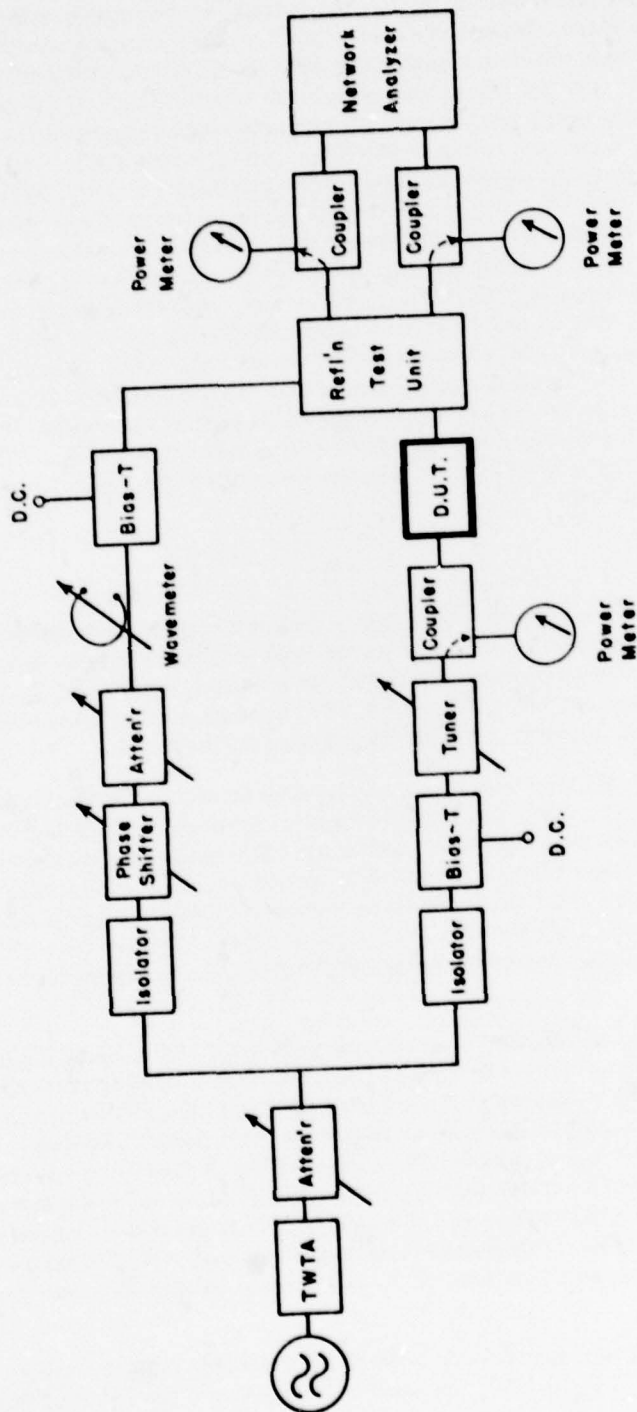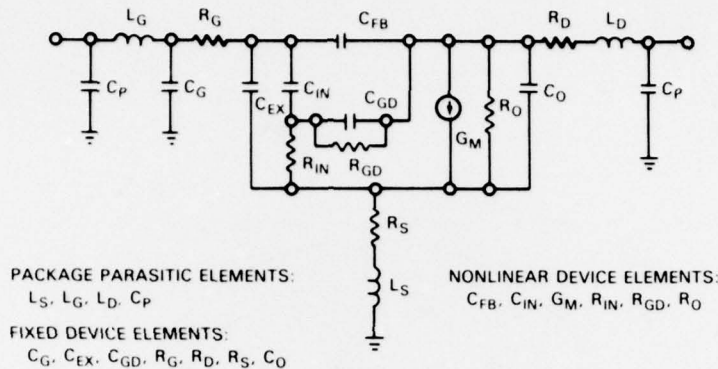
Fig. 3 — Model topology of a GaAs FET

in predicting power gain contours [18,19]. Model-predicted gain contours are compared to the experimental "load-pull" characteristics of this device in Figs. 4 and 5; the experimental load-pull test system used was described in Fig. 2. Excellent agreement between experimental results and model predictions was obtained. This experimentally verified quasi-static technique has been successfully employed for simulating, in the time-domain, non-linear performance of both FET power amplifiers and FET oscillators. The model can, however, easily be reformulated for direct application in frequency-domain problems, such as in the optimization of intermodulation distortion in linear amplifiers. The ability of this model to accurately predict power-gain under complex load conditions demonstrates its value for power amplifier development. Optimum large-signal conditions, as set by specified dynamic ranges or output power-gain levels, can be analytically determined over extended frequency ranges. The technique can assist in the realization of the full potential of power GaAs FET performance; and the important aspects of the output load characteristics when designing for low intermodulation levels or optimum power performance can be assessed. Gain and efficiency characteristics can be analyzed together with expected performance trade-offs based on small- and large-signal design approaches.

Analytical models under development will complement the quasi-static modeling technique. Expressions will be available to relate the physical and structural device parameters to each model-element value [14]. An alternate analytical model [13] will provide explicit expressions relating device terminal IV characteristics to the device parameters.

The most accurate broadband power GaAs MESFET amplifier designs are derived from complete device characterization through laboratory measurements. These measurements provide the requirements for accurately modeling intended device structures. Analytical models, providing insight into the influence of device parameters on amplifier performance, will be valuable in the realization of optimum device structures for given modes of operation. In addition, they will be useful for accurately modifying (scaling) quasi-static models, which simulate actual device structures, to accommodate changes in device parameters. This will provide a method for assessing anticipated improvements in device performance resulting from device material or geometry changes.
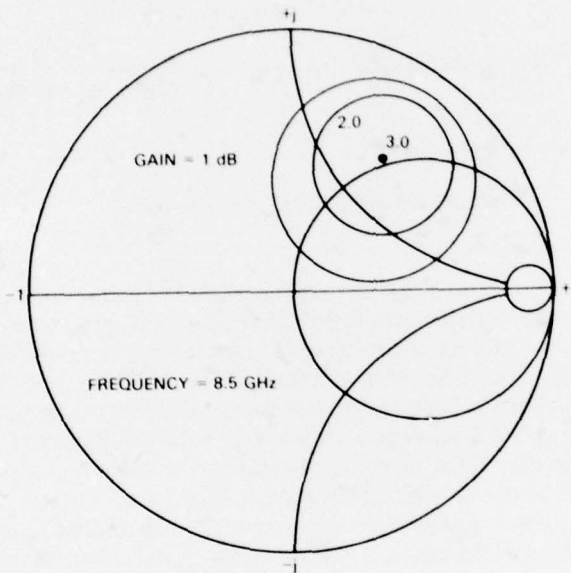
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Fig. 4 — Measured and predicted small-signal constant gain contours at 8.5 GHz plotted in the output load reflection plane (input port untuned; measured and predicted curves coincide). Device: GaAs MESFET, 600 μm (ℓ_w) × 1.7 μm (ℓ_g). Bias: 6.0 VDC (V_{DS}), - 2.0 VDC (V_{GS}).
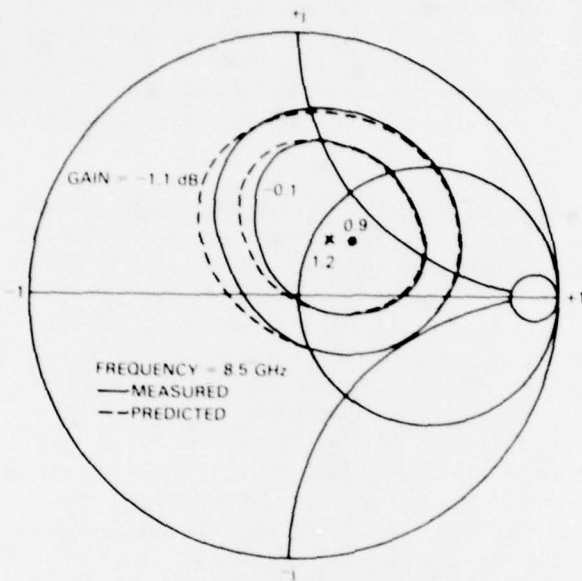
Fig. 5 — Measured and predicted constant power-gain contours at 8.5 GHz plotted in the output load reflection plane (input port untuned). Input power: 20 dBm. Device: GaAs MESFET, 600 μm (ℓ_w) $\times$ 1.7 μm (ℓ_g). Bias: 6.0 VDC (V_{DS}), -2.0 VDC (V_{GS}).

The methods described above for characterizing and simulating full device performance are valuable tools for implementing successful wideband GaAs MESFET power amplifier designs. Designs employing these techniques, experimental or analytical, presently require large-signal device characterization at multiple frequencies over the desired range of operation. This form of characterization may be very time consuming and costly when "load-pulling" laboratory measurements and model simulations by computer analysis programs are involved. An alternative approach combining model simulation techniques with only single-frequency large-signal analysis is being studied at NRL [20]. This will greatly simplify the design procedure.

Measurement Results

Laboratory measurements which include small- and large-signal tests were performed on state-of-the-art 300-μm (ℓ_w) $\times$ 1-μm and 0.8-μm (ℓ_g) cell structures. These measurements were made on both single- and dual-cell configurations. Small-signal, S-parameter measurements were taken in the 2- to 12-GHz range using an HP Automatic Network Analyzer and the described test fixture (Fig. 1) for the device under test. Device S-parameters were then de-embedded from the fixture parameters [8]. Measured S-parameters of the single- and dual-cell 300- $\times$ 0.8-μm devices are plotted in Figs. 6 and 7. The values of the elements in the circuit-type model were set to fit the model to measured S-parameters; these fitted

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values of the model elements are listed in Table 1. The model simulation of the device S-parameters are included in Figs. 6 and 7 not only in the measured 2- to 12-GHz band but also extended to 18 GHz. The development of the 6- to 18-GHz amplifier designs reported herein utilized model simulated S-parameters (small-signal). Although small-signal design concepts were used, the extension of the basic techniques to large-signal designs will be discussed.
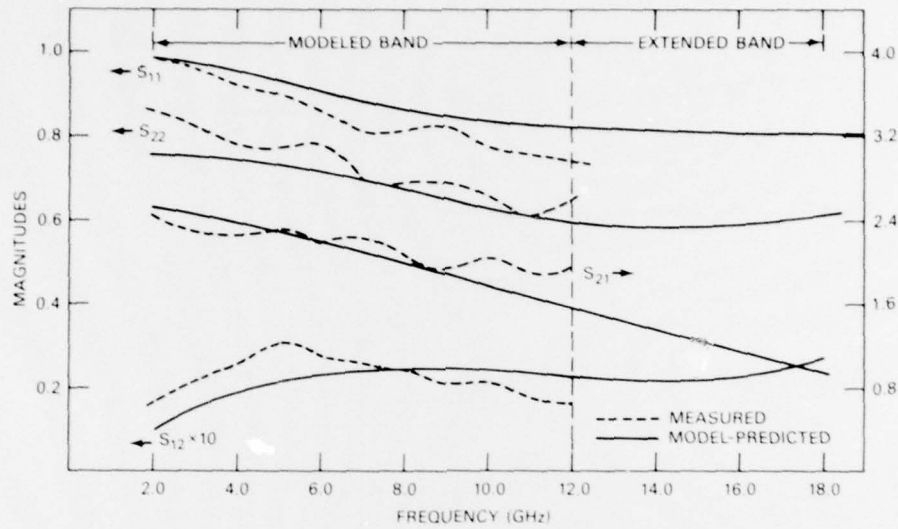
Important factors governing the design of power amplifiers are gain, linearity, and power performance. These factors will dictate large- vs small-signal amplifier design philosophy. Specified power-gain performance levels are optimally set by the output load impedance. Tests have shown that for increasing output power levels the output load impedance for maximum power-gain approaches the center of the Smith Chart (50 Ω). The power dependence of the input matching conditions is found to be minimal. For illustration, the output load dependence can be seen in the measured and predicted small- and large-signal power-gain contours in Figs. 4 and 5 for the 600- $\times$ 1.7-μm device. The optimum output load impedance changes from the small-signal value of 49 + $j75$ Ω (Fig. 4) to 60 + $j30$ Ω for an output power of +20.9 dBm. From these power contours, it is seen that a 1-dB improvement in power-gain can be realized at +20.9-dBm power output by matching for the large-signal as opposed to the small-signal load condition. When tuned for maximum small-signal gain, the device is operating into 3 dB of gain compression at the +20.9-dBm output power level. Operating into a matched load condition at +20.9 dBm, the device is at approximately 1 dB of gain compression with a reduction in small-signal gain of 1 dB. It is significant to note that the dynamic range or linearity of device performance would also be significantly improved at a sacrifice of only 1 dB in small-signal performance. These results were obtained with the input device port in a 50-Ω system (untuned).

Figure 8 illustrates measured power-gain responses of the 300- $\times$ 1-μm device for two different output load conditions at 8.5 GHz. These measurements were taken using the active load-pulling technique. The input port to the device was maintained in a fixed 50-Ω system (untuned), and the bias was set at a drain-to-source voltage of 8.0 VDC and a gate-to-source voltage of $-$1.0 VDC. At this bias point the device was operating at approximately one-half I_{DSS} (55 mA), as seen from the curves of Fig. 9. Curve A of Fig. 8 depicts the power response under the optimum, small-signal, output load impedance. The associated reflection coefficient is $0.7 < 50°$. The 1-dB power compression point for this small-signal load condition is shown to occur at an output power level of approximately +19 dBm. An output reflection coefficient of $0.5 < 50°$ increases the 1-dB compression point output power level to +20.7 dBm, as demonstrated by the response of curve B. This improved power gain performance of 1.7 dB was achieved with a reduction in the small-signal gain of approximately 0.5 dB. The associated response of the power-added efficiency is plotted in Fig. 10. The maximum power added efficiency under the small-signal load condition is 23%; an improvement to 31% is obtained with the large-signal matching condition.

3. BROADBAND GaAs POWER AMPLIFIER DESIGN CONCEPTS

An integrated approach to the design of broadband GaAs power amplifiers using both analytical and computer-aided design (CAD) techniques has been developed and applied to the 6- to 18-GHz GaAs MESFET amplifiers. (see Appendix A). The design is based on

(a)

(b)

Fig. 6 — Measured and predicted S-parameters for a single-cell GaAs MESFET. (a) magnitudes vs frequency, (b) phase angles vs frequency. Cell size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g). Bias: 6.0 VDC (V_{DS}), 0.0 VDC (V_{GS}).

(a)

(b)

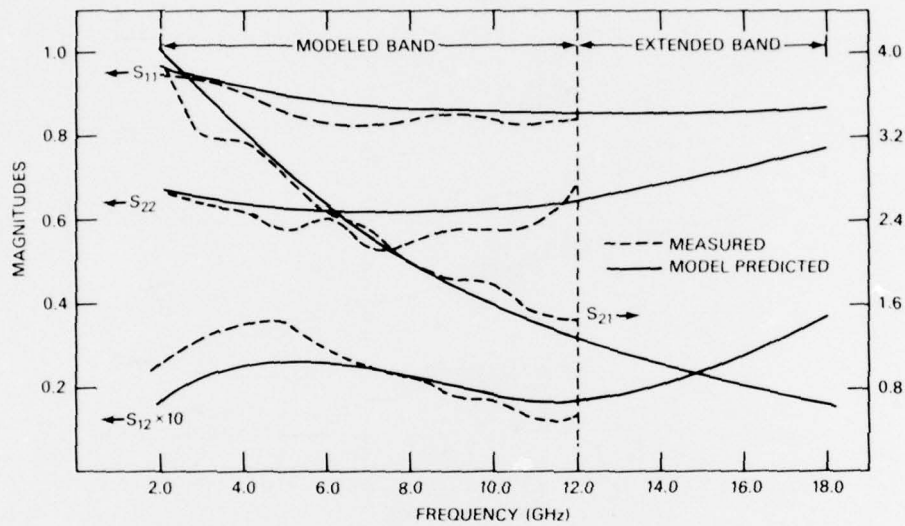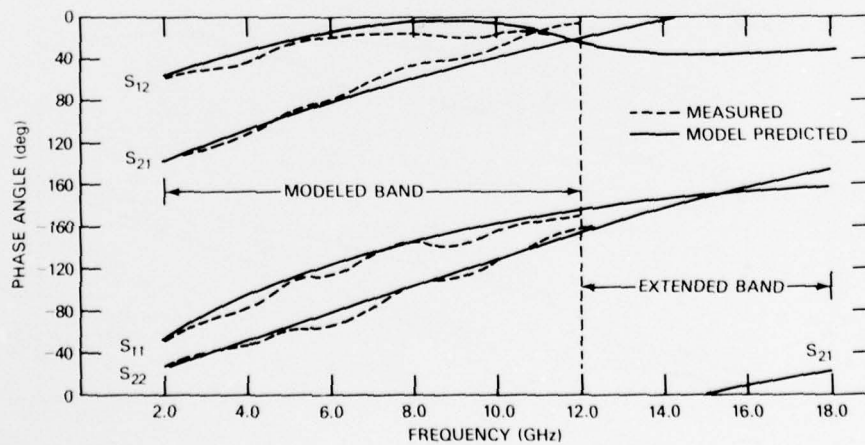Fig. 7 — Measured and predicted S-parameters for a dual-cell GaAs MESFET. (a) magnitudes vs frequency, (b) phase angles vs frequency. Cell size: 300 μm (ℓ_w) X 0.8 μm (ℓ_g). Bias: 6.0 VDC (V_{DS}), 0.0 VDC (V_{GS}).

Table 1 — Element Values of Circuit-Type GaAs MESFET Model.*
Cell Size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g).
Bias: 6.0 VDC (V_{DS}), 0.0 VDC (V_{GS})

Element		Configuration	
Type	Symbol	Single-Cell	Dual-Cell
Package Parasitic	L_S	0.018 nHy	0.019 nHy
	L_G	0.27	0.18
	L_D	0.43	0.37
	C_P	0.018 pF	0.018 pF
Fixed Device	C_G	0.12 pF	0.16 pF
	C_{EX}	0.035	0.071
	C_{GD}	—	—
	R_G	5.0 ohms	2.6 ohms
	R_D	4.1	2.2
	R_S	0.65	0.30
	C_O	0.18 pF	0.30 pF
Nonlinear Device	C_{FB}	0.0085 pF	0.018 pF
	C_{IN}	0.24	0.48
	G_M	30 mmho's	57 mmho's
	R_{IN}	5.7 ohms	3.0 ohms
	R_{GD}	—	—
	R_O	369.	275

*For circuit description see Fig. 3.

Fig. 8 — Measured power-gain response characteristics of a single-cell GaAs MESFET. Cell size: 300 μm (ℓ_w) $\times$ 1.0 μm (ℓ_g). Bias: 8.0 VDC (V_{DS}), −1.0 VDC (V_{GS}).

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Fig. 9 — Measured static (DC) I_{DS}-V_{DS} curves of a single-cell GaAs MESFET.
Cell size: 300 μm (ℓ_w) $\times$ 1.0 μm (ℓ_g).
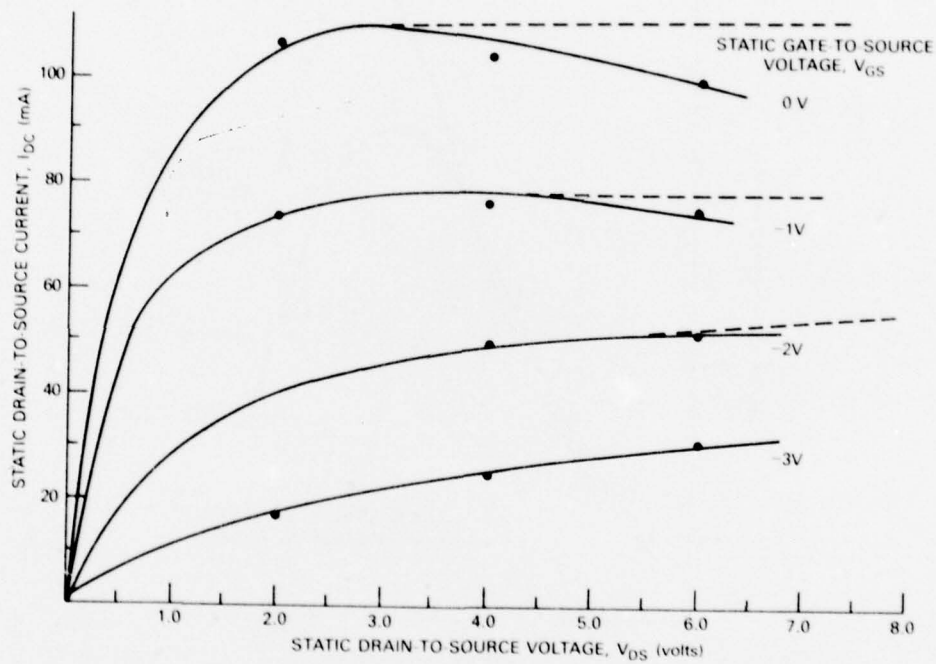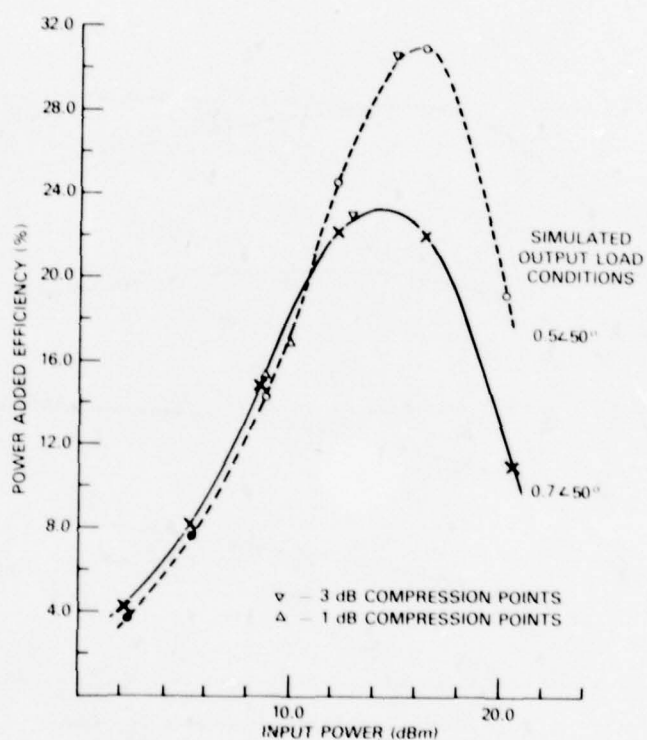
Fig. 10 — Measured power-added efficiency of a single-cell GaAs MESFET. Cell size: 300 μm (ℓ_w) $\times$ 1.0 μm (ℓ_g). Bias: 8.0 VDC (V_{DS}), -1.0 VDC (V_{GS}).

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measured device characteristics and distributed equivalent circuits. The equivalent circuits are used first to predict the gain — bandwidth limitations [21,22]. Based on the equivalent circuits, broadband distributed matching networks are synthesized for some prescribed gain slope across the specified frequency band [23,24].

As discussed in Section 2, the state-of-the-art Texas Instrument single- and dual-cell MESFETs have been characterized by measuring the small-signal scattering parameters and deriving device equivalent circuits to fit the measured data up to 12 GHz. The device equivalent circuits are then used to smooth and extend the scattering parameters to 18 GHz. Subsequently, the smoothed, extended scattering parameters of the devices from 6 to 18 GHz are used to derive unilateral lumped and distributed equivalent circuits. These equivalent circuits and the corresponding optimum gain — bandwidth limitations for both the single- and dual-cell devices are presented in Figs. 11 and 12 and Tables 2 and 3.

The optimum gain — bandwidth limitations derived for the single- and dual-cell MESFETs establish the inherent broadbanding capabilities of these devices. The distribution of the gain tapers in the input and output matching networks is an important design consideration. For power MESFET amplifier designs, the output matching networks must be flat to provide for maximum power output across the prescribed frequency band. Thus the intrinsic 6 dB/octave gain roll-off of the individual FETs must be compensated by the input matching network.

Synthesis of Distributed Matching Networks

The distributed commensurate-line matching networks to be synthesized consist of an arbitrary cascade of unit elements and open-circuited and short-circuited series or shunt stubs, with the total number of elements, n, constrained to be an even number. The transfer function of such a network in the Richards [25] transformation domain is given by

$$G_M(\Omega^2) = \frac{\Omega^{2m}(1 + \Omega^2)^q}{P_n(\Omega^2)} , \qquad (1)$$

where $P_n(\Omega^2)$ is an nth-degree polynomial in Ω^2 and $\Omega = \tan \omega T$ with T being the delay length of the commensurate transmission lines. In Eq. (1), m is the number of "high-pass" sections corresponding to series-open stubs or shunt-shorted stubs and $(n-m-q)$ is the number of "low-pass" sections corresponding to series-shorted stubs or shunt-open stubs. The parameter q is the number of unit elements corresponding to the cascaded series transmission lines.

In Eq. (1), the polynomial $P_n(\Omega^2)$ has been derived to provide a maximally flat or equiripple approximation to the ideal tapered-magnitude gain function for the distributed case given by

$$G_I(x) = \left\{ \frac{1}{\omega_h T} \tan^{-1} \sqrt{x} \right\}^{2\alpha}, \qquad (2)$$

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All Lines ℓ = λ/8 at 18 GHz

Z_{iL} = 25.25Ω Z_{oL} = 41.82Ω
Z_{iC} = 15.74Ω Z_{oC} = 36.72Ω
R_i = 5.26Ω R_o = 195.32Ω

Fig. 11 — Distributed equivalent circuit of Texas Instruments, Inc. single-cell, high-power MESFETs (6-18 GHz)

Table 2 — Optimum Gain — Bandwidth Limitations of Texas Instruments, Inc. Single-Cell High-Power MESFETs (6-18 GHz)

Gain Slope (dB/oct)	Input Limitation (Z_{iC}) (dB)	Output Limitation (Z_{oC}) (dB)
0 (Flat)	Gain Red. = −2.71	Gain Red. = −0.96
3	Gain Red. = −0.48	Gain Red. = 0
6	Gain Red. = 0	Gain Red. = 0

All Lines Are ℓ = λ/8 at 18 GHz

$Z_{iL} = 18.81\Omega$ $Z_{oL} = 39.15\Omega$

$Z_{iC} = 8.49\Omega$ $Z_{oC} = 21.74\Omega$

$R_i = 3.85\Omega$ $R_o = 131.95\Omega$

Fig. 12 — Distributed equivalent circuit of Texas Instruments, Inc. dual-cell, high-power MESFETs (6-18 GHz)

Table 3 — Optimum Gain — Bandwidth Limitations of Texas Instruments, Inc. Dual-Cell High-Power MESFETs (6-18 GHz)

Gain Slope (dB/oct)	Input Limitation (Z_{iC}) (dB)	Output Limitation (Z_{oC}) (dB)
0 (Flat)	Gain Red. = −1.89	Gain Red. = −1.21
3	Gain Red. = 0	Gain Red. = −0.10
6	Gain Red. = 0	Gain Red. = 0

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where $x = \Omega^2$, α is the gain-taper parameter, and ω_h is the radian frequency at the high end of the frequency band. Note that Eq. (2) is the ideal tapered-gain characteristic in the real frequency variable ω. Since commensurate transmission line networks are periodic, for the tapered-magnitude gain functions, the line length must be strictly less than a quarter-wavelength at ω_h.
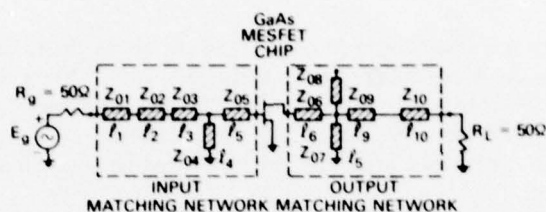
Broadband GaAs MESFET Amplifier Designs

Broadband single-stage GaAs MESFET amplifiers have been designed as shown in Fig. 13. The amplifiers are designed using the Texas Instruments single- and dual-cell configurations, and the microstrip amplifier topology and element values are derived by direct distributed synthesis with commensurate lines. The calculated amplifier gain responses for the prescribed 6- to 18-GHz frequency band are presented in Fig. 14. For the single-cell device, the optimized gain is 6.0 dB with a passband ripple of ± 0.45 dB across the entire 6- to 18-GHz band. The maximum available gain for the single-cell device is 6.4 dB at 18 GHz based on the measured scattering parameters. For the dual-cell device, the optimized gain is 5.5 dB with a gain flatness of ± 0.45 dB across the prescribed frequency band of 6 to 18 GHz.

All the matching networks are initially synthesized for equiripple characteristics with a prescribed gain slope. Computer optimization is used only to correct for the uni-lateral approximation and inaccuracies in the distributed equivalent circuit models.

The design procedure described for the small-signal GaAs MESFET amplifiers must be modified for power amplifier design. A completely rigorous design requires large-signal characterizations of the MESFETs. The design procedure presented previously is still valid with appropriate modifications. The output matching network must first be designed to provide for maximum power output. The optimum gain — bandwidth limitations can still be calculated based on the large-signal equivalent circuit of the device. The reactive constraint imposed by the output of the device will become less restrictive than that predicted by the small-signal equivalent circuit. As an initial approximation, we can reduce the equivalent output resistance R_o as shown in Fig. 11 by an appropriate factor and recalculate the output gain — bandwidth limitation. Using this approximation, we first synthesize a flat output matching network. By inserting the device equivalent circuit of the FET, we can calculate the effective input impedance or modified S_{11} of the MESFET. Using this calculated result, we can recalculate the effective input gain — bandwidth limitation and required gain slope of the input matching network. This network is then synthesized for the prescribed gain slope and reactive constraint. In the final optimization, the output matching network is constrained to maintain a flat match, and the input matching network is varied to provide gain tapering.

4. AMPLIFIER PERFORMANCE AND ANALYSIS

The following discussion presents the design, fabrication, and performance measurements of single-ended, 6- to 18-GHz, GaAs power MESFET amplifiers. These amplifiers employ state-of-the-art GaAs MESFETs with a single-cell size of 300-μm gate width (ℓ_w)

I. 1 CELL MESFET AMPLIFIER (INITIAL LINE LENGTH = λ/8 AT 18 GHz)

$Z_{01} = 25\Omega$, $\ell_1 = 45''$	$Z_{06} = 40\Omega$, $\ell_6 = 35''$
$Z_{02} = 55\Omega$, $\ell_2 = 45''$	$Z_{07} = 70\Omega$, $\ell_7 = 45''$
$Z_{03} = 15\Omega$, $\ell_3 = 68''$	$Z_{08} = 18\Omega$, $\ell_8 = 45''$
$Z_{04} = 98\Omega$, $\ell_4 = 50''$	$Z_{09} = 55\Omega$, $\ell_9 = 45''$
$Z_{05} = 42\Omega$, $\ell_5 = 12''$	$Z_{10} = 28\Omega$, ℓ_{10} = 45''

II. 2 CELL MESFET AMPLIFIER

$Z_{01} = 25\Omega$, $\ell_1 = 45''$	$Z_{06} = 27\Omega$, $\ell_6 = 45''$
$Z_{02} = 44\Omega$, $\ell_2 = 45''$	$Z_{07} = 69\Omega$, $\ell_7 = 45''$
$Z_{03} = 12\Omega$, $\ell_3 = 61''$	$Z_{08} = 21\Omega$, $\ell_8 = 45''$
$Z_{04} = 180\Omega$, $\ell_4 = 98''$	$Z_{09} = 62\Omega$, $\ell_9 = 45''$
$Z_{05} = 9\Omega$, $\ell_5 = 11''$	$Z_{10} = 26\Omega$, $\ell_{10} = 45''$

Fig. 13 — 6- to 18-GHz GaAs MESFET amplifier configuration using single- and dual-cell 300-μm (ℓ_w) $\times$ 0.8-μm (ℓ_g) MESFET chips
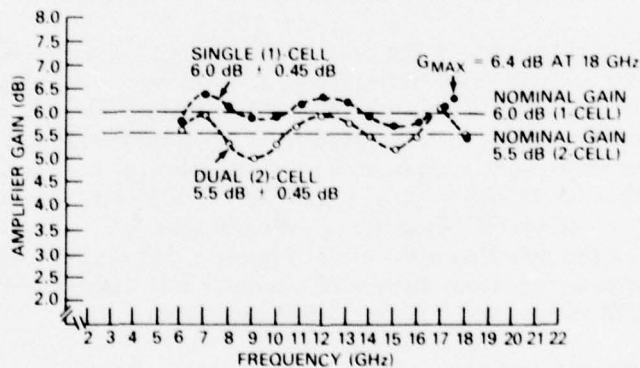

Fig. 14 — Calculated 6- to 18-GHz band GaAs MESFET amplifier responses for Texas Instruments, Inc. single-cell and dual-cell 300-μm (ℓ_w) $\times$ 0.8-μm (ℓ_g) FETs

and 0.8-μm gate length (ℓ_g). Devices in single- and dual-cell configurations were used. As was previously stated, the amplifier designs are based upon small-signal characterization and modeling. They were developed to achieve maximum small-signal gain across the 6- to 18-GHz frequency band.

For flat amplifier response characteristics, gain tapering must be provided by the matching networks to the input and/or output device ports. This is to correct for the inherent gain slope characteristics of the GaAS FET devices. Amplifiers designed for optimum power-gain performance constrain the gain tapering to the device input port. A flat match response at the output port must be provided to achieve optimum power-gain transfer characteristics.

The S-parameters for both the single-and dual-cell configurations previously specified were measured using the Automatic Network Analyzer in the 2- to 12-GHz band. The S-parameters were determined at a bias condition of 6.0 VDC, drain-to-source voltage, and 0.0 VDC, gate-to-source voltage. This bias condition was established to obtain a high value of small-signal gain and not for optimum power gain. A gate-to-source voltage providing approximately one-half I_{DSS} would be more suitable if maximum saturated power gain is desired. A computer-aided optimization program (COMPACT) was used to obtain the circuit-type model element values listed in Fig. 3 for both device structures (single and dual cells). The values were determined by fitting the model-predicted S-parameters to the measured S-parameters. Plots of these parameters were previously discussed and are given in Figs. 6 and 7. Required sets of S-parameters in the 6- to 18-GHz range were determined from simulations using the developed models.

The approach used to establish the basic amplifier designs and projections given in this section has been fully discussed in Section 3. The following outlines this approach. Equivalent distributed circuit-type models (Fig. 11) simulating the input and output port characteristics of each device were determined from the developed sets of 6- to 18-GHz S-parameters. From these models, input and output matching networks were synthesized. The input networks were defined to provide a positive 6-dB/octave insertion loss slope, and a matched condition was established at the upper-band edge. Each output network was synthesized to give a flat match over the band of interest. The complete amplifier topology and element values as derived from distributed synthesis with commensurate lines is given in Fig. 13 for both the single- and dual-cell devices (see Section 3).

The final single- and dual-cell amplifier designs were modifications of the synthesized networks previously described. Design development commenced with these networks; however, the output network was modified to contain a single stub element for ease of realization. An additional series-transforming section was added to the output section, and computer optimization was used to fit the amplifier response to a specified gain and gain-flatness. The starting matching circuit element values were taken from the synthesized topologies. The final design allowed both the individual line lengths and impedances to vary. To correct for junction effects between line elements, lumped L, C elements were inserted [26]; the values of these elements were determined from the final optimized line impedances. With these lumped elements included in the final circuit topologies, the line length of each transforming element was refitted to achieve the defined gain frequency response. The final amplifier topology and the computer-fitted element parameters for the

single- and dual-cell devices are given in Fig. 15 and Table 4. Computer-predicted gain response characteristics for each amplifier are given in Figs. 16 and 17.
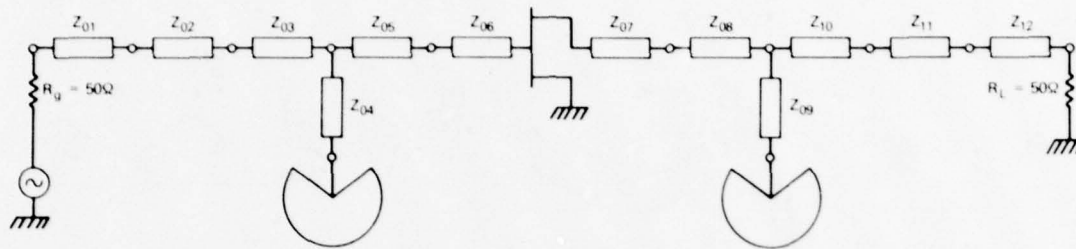

Fig. 15 — 6- to 18-GHz GaAs power MESFET amplifier topology.
Cell size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g).

Table 4 — 6- to 18-GHz GaAs Power MESFET Amplifier Computer-Fitted
Element Parameters. Cell Size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g).

Line Parameters		Input Matching Network						Output Matching Network					
		Z_{01}	Z_{02}	Z_{03}	Z_{04}	Z_{05}	Z_{06}	Z_{07}	Z_{08}	Z_{09}	Z_{10}	Z_{11}	Z_{12}
Single-Cell Amplifier	Impedance (Ω)	25.9	55.9	15.0	100.0	15.0	41.8	35.0	18.5	85.1	18.5	45.0	36.0
	Length (Deg. at 18 GHz)	42.5	37.9	59.5	56.0	10.0	10.0	38.7	10.0	40.3	42.4	43.5	88.0
Dual-Cell Amplifier	Impedance (Ω)	23.3	42.9	15.0	15.0	15.0	40.0	40.0	15.0	71.3	15.0	34.2	41.9
	Length (Deg. at 18 GHz)	41.7	51.0	49.5	140.1	12.0	5.0	5.0	29.9	63.0	9.7	53.3	81.4

Single-ended amplifiers comprised of the circuit descriptions given in Fig. 15 were fabricated and tested. The input and output matching networks were formed on 15-mil (0.38-mm)-thick fused quartz substrates. The substrate selection permitted the use of low-impedance transforming line elements without the formation of higher order modes at the upper-band edge. Gate and drain DC bias connections were made through RF short-circuit stub elements; RF shorts were provided by radial line elements. A photograph depicting the amplifier topology is given in Fig. 18.

Measured DC-IV characteristics of two single-cell devices are given in Figs. 9 and 19. One-half I_{DSS} for these devices are 55 mA and 40 mA, respectively; the single-cell amplifier described in this section employed the latter device. Operating these devices at a drain
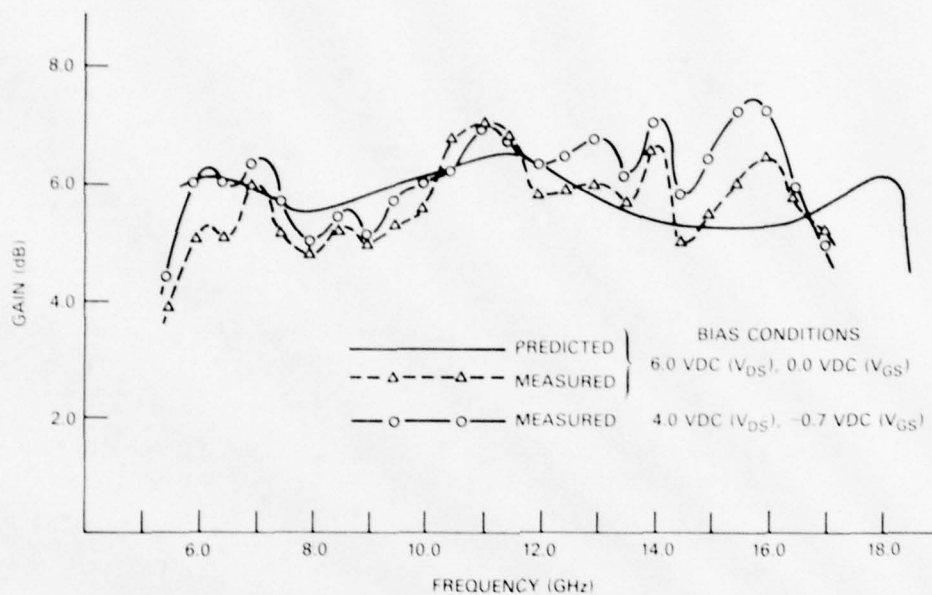
Fig. 16 — Measured and predicted small-signal gain response of a single-cell
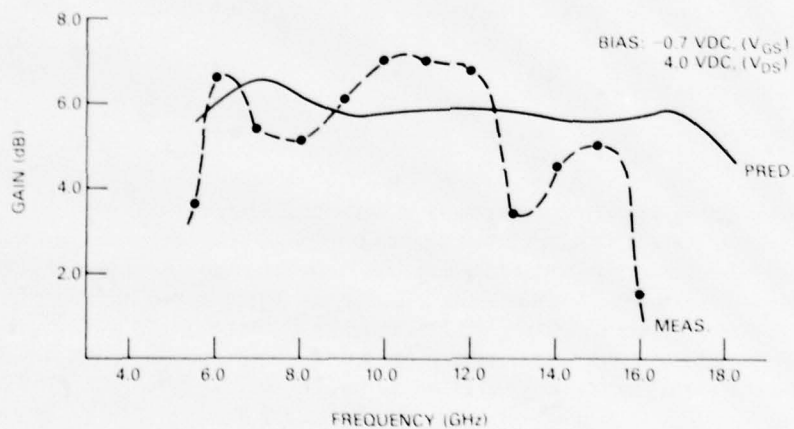GaAs MESFET amplifier. Cell size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g).

Fig. 17 — Measured and predicted small-signal gain response of a dual-
cell GaAs MESFET amplifier. Cell size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g).
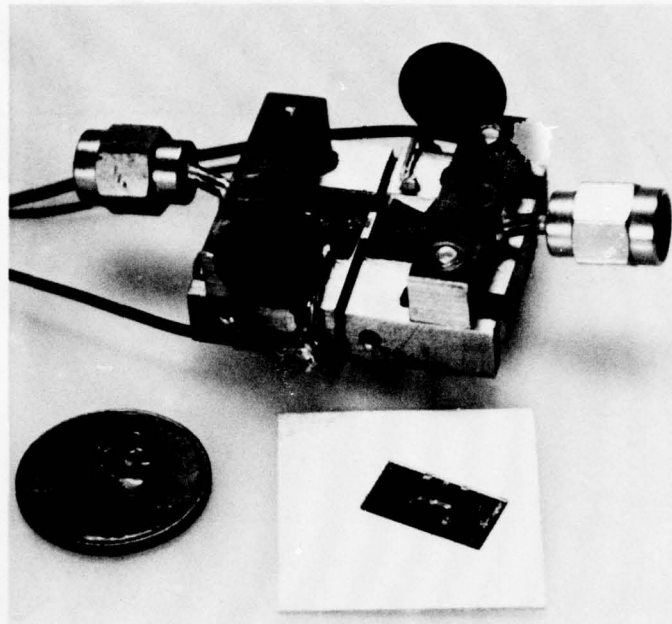
22

Fig. 18 — Single-ended GaAs MESFET amplifier

bias V_{DS} of 6.0 VDC, the projected output powers are 22.2 and 20.8 dBm, respectively. The fabricated dual-cell amplifier employed a device whose characteristics are partially given in Fig. 20. Operating this device at one-half I_{DSS} and a drain bias of 6.0 VDC, an achievable output power of 24.8 dBm is projected.

The measured characteristics of the single-cell amplifier are given in Figs. 16 and 21-23. Figure 16 depicts the gain responses taken at the designated bias conditions. In the figure, comparisons are made between the measured gain and the computer-predicted response based upon the measured set of S-parameters for a bias of 6.0 VDC (V_{DS}) and 0.0 VDC (V_{GS}). The sharp roll-off in the measured gain response at the low end of the frequency band is attributed to the low-pass filter response characteristics of bias networks. Measured power-gain response of the single-cell amplifier is illustrated in Figs. 21 and 22 for bias conditions of 4.0 VDC (V_{DS}), −0.7 VDC (V_{GS}), and 6.0 V_{DC} (V_{DS}), −0.7 VDC (V_{GS}), respectively. Included in Figs. 21 and 22 are the power gains at the 1- and 2-dB compression points. The presented amplifier characteristics are from measurements with original (unmodified) matching circuit elements. The derivation of the element parameters was based upon small-signal S-parameters. Improved power performance was achieved by laboratory tuning of the output matching circuit; a fixed metallized tab was included to modify the line impedance of the last output circuit element. Operating at the specified bias conditions, the modified amplifier has the measured power-gain characteristics illustrated in Fig. 23. The associated power-added efficiency performance is included. It is noted that improved power operation was achieved by improving the output impedance match established from the small-signal design.

Fig. 19 — Measured static (DC) I_{DS}-V_{DS} curves of a single-cell GaAs MESFET.
Cell size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g).

Fig. 20 — Measured static (DC) I_{DS}-V_{DS} curves of a dual-cell GaAs MESFET.
Cell size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g).

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Fig. 21 — Single-ended GaAs MESFET amplifier power response. Device: single-cell GaAs MESFET. Cell size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g). Bias: 4.0 VDC (V_{DS}), -0.7 VDC (V_{GS}).

Fig. 22 — Single-ended GaAs MESFET amplifier power response. Device: single-cell GaAs MESFET. Cell size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g). Bias: 6.0 VDC (V_{DS}), -0.7 VDC (V_{GS}).

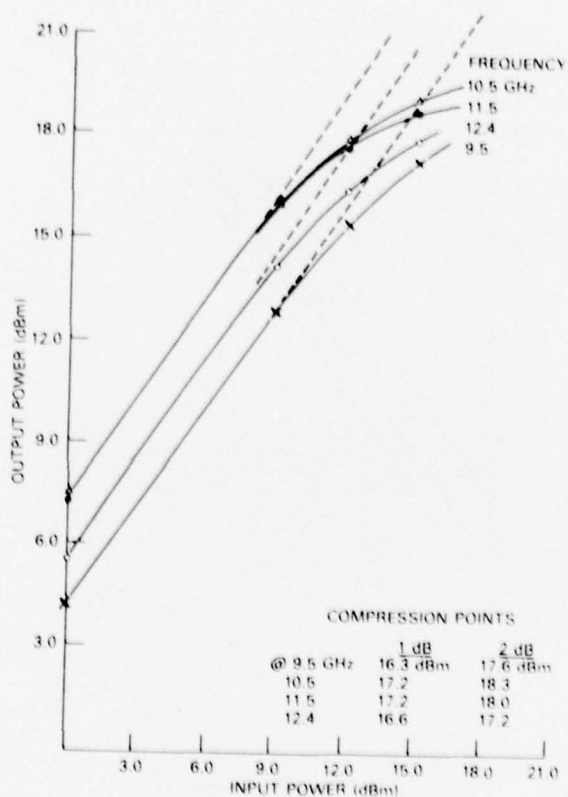Fig. 23 — Single-ended GaAs MESFET amplifier power response. Device: single-cell GaAs MESFET. Cell size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g). Bias: curve A, 6.0 VDC (V_{DS}), -1.25 VDC (V_{GS}); curve B, 7.0 VDC (V_{DS}), -1.5 VDC (V_{GS}).

A dual-cell amplifier was developed and fabricated similarly to the single-cell amplifier. This design was also based on small-signal characterization. Figures 17 and 24 illustrate the measured performance of this amplifier. The depicted gain and power-response characteristics were measured with unmodified matching circuit elements. The gain fall-off at the low end of the band results from loading of the DC bias networks. Improved gain response at the upper-band edge is expected through a reduction in bond wire inductances to the gate and drain pads of the device. Single-wire interconnects were used between each cell pad and the external circuits. Multiple bond wires to the device pads reducing the effective lead inductances were not employed due to assembly equipment limitations. Enhancement of the power-gain performance can be realized through the implementation of the large-signal characterization and design techniques presented in this report.
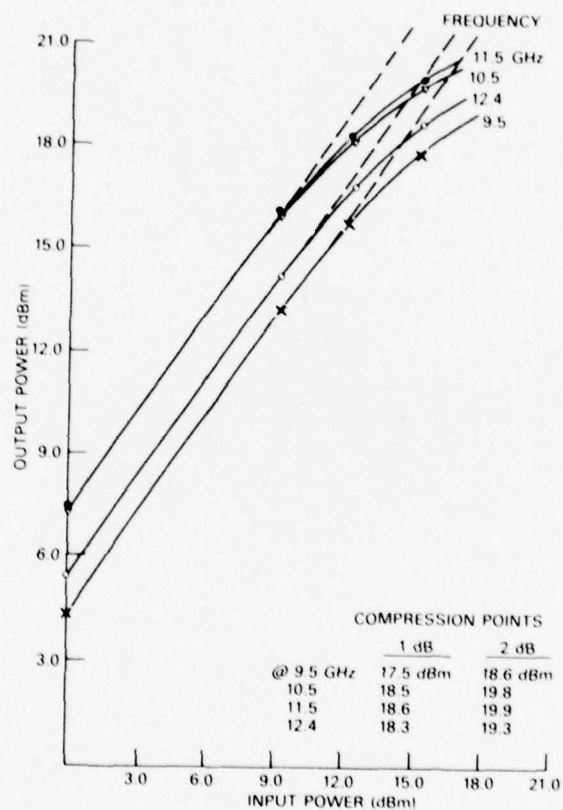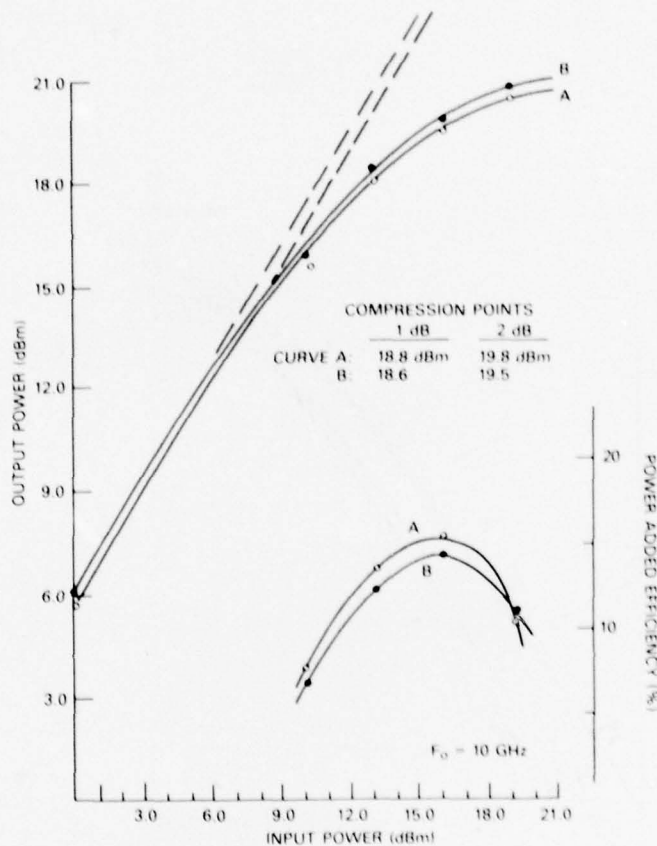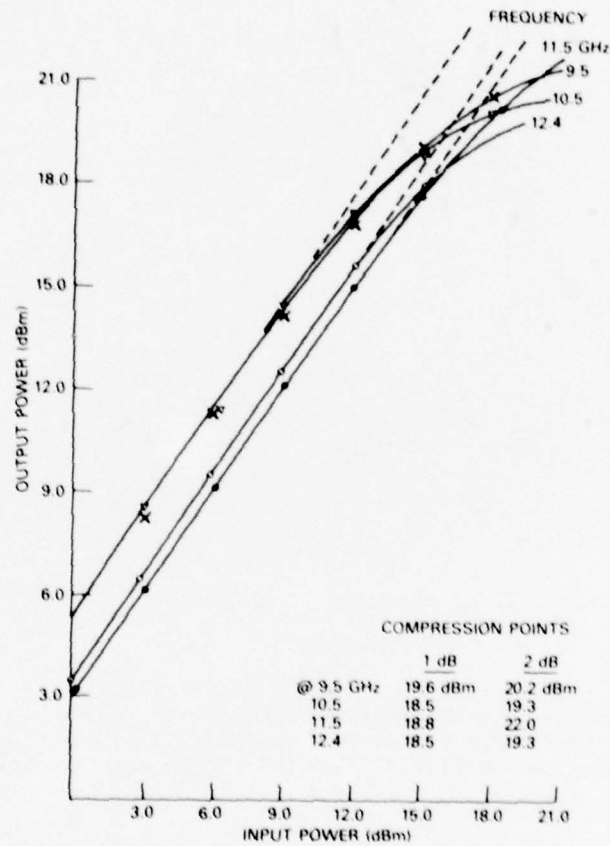
27

Fig. 24 — Single-ended GaAs MESFET amplifier power response. Device: dual-cell GaAs MESFET. Cell size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g). Bias: 6.0 VDC (V_{DS}), -0.7 VDC (V_{GS}).

The methods described can be used in either small- or large-signal amplifier designs. However, during the initial phases of this effort, the technique for developing a large-signal circuit-type model suitable for use in amplifier design was not complete. Thus, the amplifier development discussed in this report was restricted to the use of small-signal device models and, therefore, the results do not fully reflect optimum power-gain levels.

5. CONCLUSIONS

Techniques and tools for implementing the development of power GaAs MESFET amplifiers have been presented, and a complete description of the synthesis of the input and output matching circuits necessary to achieve wideband performance has been given. Included were the constraints imposed on the circuits to obtain required gain flatness and output power matching conditions. The formulation of these matching circuits has been based upon the characterization and unilateral circuit modeling of the device. This circuit-type device model was developed to simulate the input and output device characteristics; it was used to establish the matching circuit topologies and starting circuit element parameters for optimization.

Ongoing device modeling efforts have been presented in the context of their influence on achieving improved device designs. These efforts are providing a more complete understanding of the relationships of physical and material device parameters to performance, thus assisting in the selection of parameter values needed to optimize device designs. Also discussed has been the adoption of these modeling techniques to provide assistance in projecting device performance. A large-signal circuit-type model of a 600-μm gatewidth (ℓ_w) $\times$ 1.7-μm gate length (ℓ_g) GaAs MESFET device has been described, which was used to predict the response of device power-gain to output-load conditions. By extending the performance of this model to cover the desired band of interest, broadband matching networks can be synthesized.

Broadband GaAs MESFET amplifier designs have been presented in frequency bands covering the full 2- to 18-GHz range. These designs, based upon small-signal device characterization and modeling, were developed to demonstrate the techniques leading to a final amplifier configuration. Single-ended amplifiers employing single- and dual-cell GaAs MESFET devices (300-μm (ℓ_w) $\times$ 0.8-μm (ℓ_g) cell size) were fabricated from the designs. Good agreement was demonstrated between the computer-predicted and measured small-signal gain characteristics of the single-cell amplifier. The output power level that was initially anticipated for the single-cell design was 23 dBm; the fact that this level was not achieved is attributed to a low device I_{DSS} and to not implementing a large-signal design. It is expected that an amplifier employing this basic device structure, but with a higher I_{DSS} and a higher operating drain-to-source voltage, can provide 23-dBm output power over the 6- to 18-GHz band. This is supported by the results of the load-pulling, power-gain performance measurements on the single-cell, 300-μm (ℓ_w) $\times$ 1-μm (ℓ_g) GaAs MESFET device. Similarly, improved performance can be anticipated from the dual-cell design.

Present broadband GaAs power MESFET amplifier design techniques require extensive laboratory measurements and do not systematically lead to optimal broadband performance. This report has presented systematic and efficient techniques.

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Appendix A

SYSTEMATIC DESIGN OF MESFET AMPLIFIERS

A systematic design approach to the development of ultra-wideband FET amplifiers is presented in this Appendix; it consists of a technique which integrates computer-aided device modeling and direct synthesis of distributed matching networks. The approach is generalized and equally applicable to designs of wideband small- and large-signal amplifiers and low-noise amplifiers. It is illustrated by the following detailed development of a 6- to 18-GHz GaAs MESFET amplifier based upon small-signal device characterization.

The amplifier design employs the Texas Instruments, Inc. 0.8-μm (ℓ_g) $\times$ 300-μm (ℓ_w) single-cell device described in the main text. A distributed equivalent circuit model of the 300-μm device and its optimum gain — bandwidth limitations are presented in Fig. 11 and Table 2. These are derived from measured small-signal scattering parameters and described in Section 3. Power amplifier input and output matching circuit constraints of 6-dB/octave gain reduction at the input and 0-dB/octave gain reduction at the output are imposed on the design (see main text). As listed in Table 2 for an input matching network with a prescribed gain slope of 6 dB/octave, the optimum gain — bandwidth limitation does not require a gain reduction to absorb the series open-circuited stub. An output gain reduction of -0.96 dB is imposed by a flat gain reduction constraint (0 dB/octave) at the output. For matching network topologies of finite complexity and whose elements are physically realizable, additional gain reduction together with a specified ripple must be chosen to satisfy the reactive constraints and achieve the required impedance transformation.

This amplifier design technique begins with the design of the output matching network. Using the direct distributed synthesis method, an output matching network of $N = 6$ with $N_L = 2$, $N_H = 1$, and $N_c = 3$* is derived to provide the flat gain response. A combination of a gain reduction of -0.9 dB and a passband ripple of $\epsilon = 0.336$ dB will yield the *exact* reactance absorption and impedance transformance across the prescribed band. The synthesized output matching network is shown in Fig. A1. Note from Fig. A1 that the reactance constraint imposed by the shunt open-circuited stub has been satisfied exactly and the impedance transformation has also been satisfied simultaneously. This is achieved by moving part of the shunt short-circuited stub (the stub with characteristic impedance of 411.16 Ω) from reference plane A to B.

After the output matching network has been designed, the element values of the equivalent input circuit (Fig. 11) of the FET are derived by using either the measured scattering parameters or the complete circuit-type model of the device in cascade with the output matching network. With the modified distributed input model, the gain — bandwidth limitation and the equivalent gain slope at the input are recalculated. It is found that the input gain slope required is approximately 6.1 dB/octave. Therefore a gain slope of 6 dB/octave is sufficient. The modified input model simulates the input device characteristics

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*N = total number of elements, N_L = number of low-pass elements, N_H = number of high-pass elements, and N_c = number of series (cascaded) unit elements.
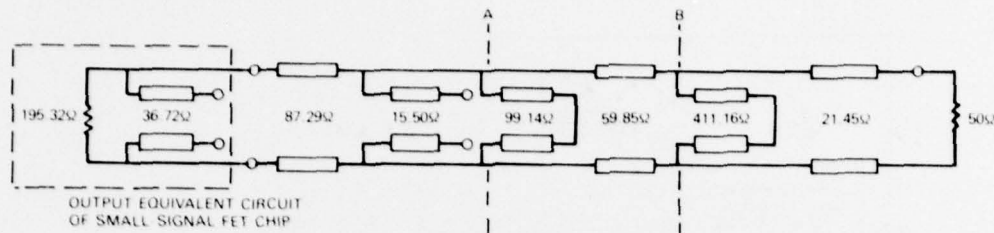
32

Fig. A1 — Synthesized output matching network for a small-signal, 6- to 18-GHz amplifier using a single-cell, 300-μm (ℓ_w) $\times$ 0.8-μm (ℓ_g) FET

and includes the nonunilateral effect of the output load. The input matching network of the amplifier is synthesized from the input circuit model. This input model is comprised of an input resistance of 4.88 Ω and a series open-circuited stub of 15.70 Ω. With a 6-dB/octave gain slope imposed at the device input port, a combination of −0.1 dB of gain reduction and a passband ripple of 0.146 dB will satisfy the input reactive constraint and the required impedance transformation. These are established by the series open-circuited stub (15.70 Ω) and the input resistance (4.88 Ω). The synthesized input matching network is shown in Fig. A2 and the exact equiripple gain response is shown in Fig. A3. The shunt stub of 740.34 Ω in Fig. A2 is a result of moving a portion of the shunt stub at reference plane A to reference plane B to satisfy the required impedance transformation.
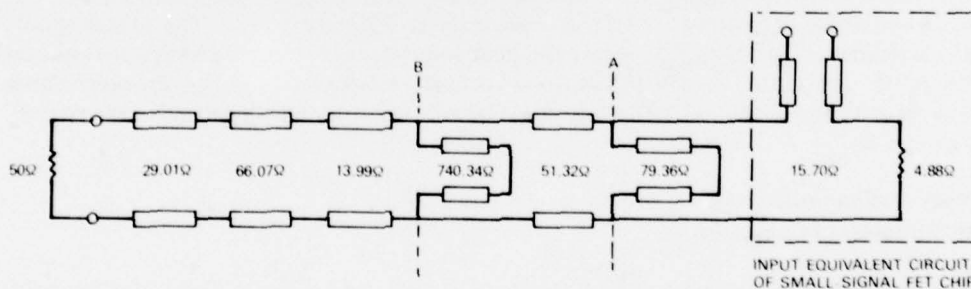

Fig. A2 — Synthesized input matching network for a small-signal, 6- to 18-GHz amplifier using a single-cell, 300-μm (ℓ_w) $\times$ 0.8-μm (ℓ_g) FET
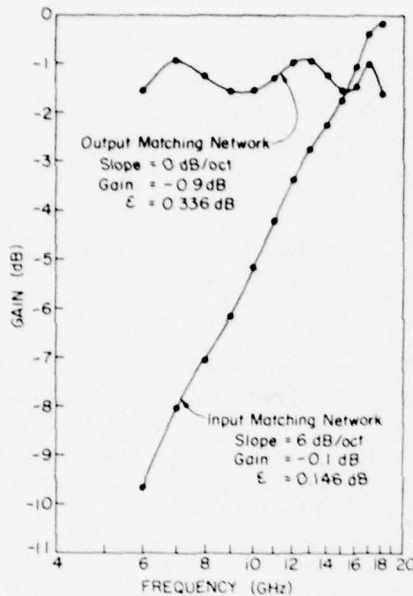
Fig. A3 — Small-signal matching networks with equiripple response characteristics for a single-cell GaAs MESFET. Cell size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g).

The design up to this stage is completely based on synthesis. The input and output matching networks are synthesized using distributed elements with *exact* equiripple gain characteristics. This initial amplifier design is evaluated by using the complete set of measured scattering parameters from the 6- to 18-GHz frequency band. The initial amplifier gain is presented in Table A1, where the gain variation across the band is approximately 5.85 dB ± 0.55 dB. Note that the initial design already satisfies gain flatness requirements for most amplifiers without using optimization. Factors contributing to the errors in this initial design are

- Modeling errors, and
- Unilateral assumption.

The error due to the unilateral assumption has been reduced by the method of remodeling the input equivalent circuit after the output matching network has been designed.

Final optimization of the amplifier gain flatness is performed by changing the characteristic impedances of the lines but keeping the length ($\ell = \lambda/8$ at 18 GHz) invariant. The optimized amplifier configuration is presented in Fig. A4 and the optimized gain and input and output VSWR is presented in Fig. A-5 and Table A2.

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Table A-1—
Initial Amplifier Gain
Response (Single Cell,
Small Signal)

Frequency (GHz)	Gain (dB)
6.0	5.3
7.0	6.3
8.0	5.7
9.0	5.3
10.0	5.6
11.0	6.0
12.0	6.4
13.0	6.3
14.0	5.9
15.0	5.6
16.0	5.7
17.0	6.2
18.0	5.7

GaAs FET CHIP

INPUT MATCHING NETWORK

OUTPUT MATCHING NETWORK

$Z_{01} = 33.3\,\Omega$

$Z_{02} = 68.6\,\Omega$

$Z_{03} = 16.9\,\Omega$

$Z_{04} = 57.6\,\Omega$

$Z_{05} = 89.5\,\Omega$

$Z_{06} = 81.7\,\Omega$

$Z_{07} = 16.6\,\Omega$

$Z_{08} = 103.3\,\Omega$

$Z_{09} = 61.3\,\Omega$

$Z_{10} = 27.1\,\Omega$
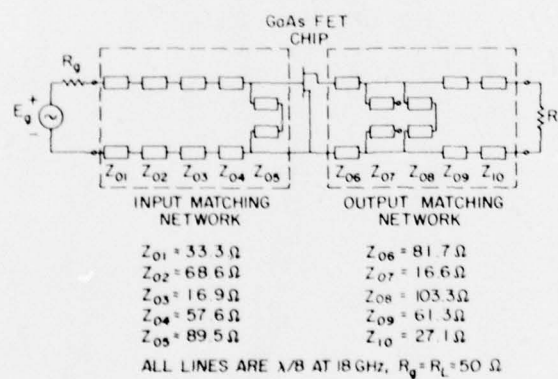
ALL LINES ARE $\lambda/8$ AT 18 GHz, $R_g = R_L = 50\,\Omega$

Fig. A4 — Small-signal 6- to 18-GHz band
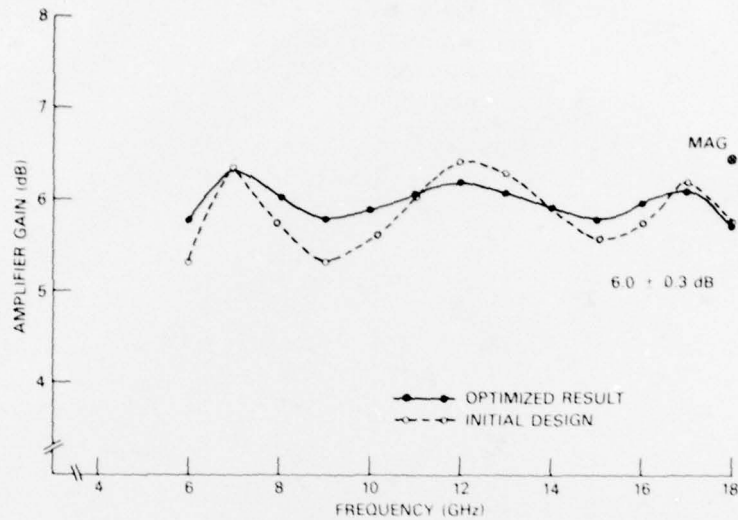GaAs FET amplifier

Fig. A5 — Calculated Texas Instruments, Inc. GaAs MESFET
small-signal amplifier response

Table A2 — Optimized Amplifier Gain Response
(Single Cell, Small Signal)

Frequency (GHz)	Gain (dB)	Input VSWR	Output VSWR
6.0	5.8	39.2	5.4
7.0	6.3	23.1	4.7
8.0	6.0	16.1	4.8
9.0	5.8	12.1	4.8
10.0	5.9	9.4	4.4
11.0	6.1	7.4	3.9
12.0	6.2	5.8	3.4
13.0	6.1	4.6	3.1
14.0	5.9	3.9	3.0
15.0	5.8	3.2	2.8
16.0	6.0	2.5	2.4
17.0	6.1	2.0	1.8
18.0	5.6	2.0	1.7

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A gain flatness of 6.0 dB ± 0.3 dB has been achieved and it is noted that the high impedance stubs at the input and output have been eliminated, but all the other element values are very close to the values from the initial design using synthesis. Also note from the optimized gain response in Fig. A5 that we have achieved a broadband gain which is very close to the maximum available gain of the device.

As previously stated, the systematic design technique described in the development of a 6- to 18-GHz GaAs MESFET amplifier using small-signal scattering parameters is equally applicable to large-signal designs. Pseudo-"large-signal" scattering parameters can be derived from the complete device circuit-type model described in Fig. 3 of the main text. At modest output power levels all elements of the model can be considered fixed or linear (derived from small-signal measurements) except the output resistance (R_o) and transductance (G_m). Output power dependence of the values of these nonlinear elements can be determined from load-pulling techniques as described in Section 2.

The following further illustrates this systematic design technique by describing the development of a 6- to 18-GHz, power GaAs MESFET amplifier. Tests have shown that the output resistance decreases by approximately one-half when operating at an output power level equivalent to 2 to 3 dB of optimum small-signal gain compression. A set of "large-signal" scattering parameters were derived from the circuit-type model of Fig. 3. The element values used are listed in Table 1; however, the output resistance is reduced in value by one-half. This approximation is used only to demonstrate the application of this generalized design technique toward the development of large-signal amplifiers. The element values of the unilateral model of Fig. 11 are derived from the scattering parameters. The input equivalent circuit consists of a resistance of 5.15 Ω and a series open-circuit stub of 18.13 Ω. The output equivalent circuit consists of a resistance of 161.29 Ω and a shunt open-circuited stub of 44.7 Ω. As expected, the output resistance has been reduced from the small-signal value of 195.32 Ω used in the previous design. The output gain — bandwidth limitation is now less restrictive as compared to the small-signal case. On the other hand, the maximum available gain has been reduced to approximately 4.5 dB at 18 GHz.

The results of the large-signal amplifier design are presented in summary form in Figs. A6 through A10 and in Tables A3 and A4. It is noted again that the initial design using synthesis alone results in an amplifier gain response with a gain variation of ±0.55 dB without using optimization. Optimized amplifier gain response for the large-signal case presented in Fig. A10 and in Table A4 shows an optimized gain of 4.1 ± 0.2 dB.

As specified, the described design techniques equally apply to low-noise amplifier designs. However, converse to power amplifier designs, the required matching network is first established for a noise match. The output characteristics of the device are then modeled.
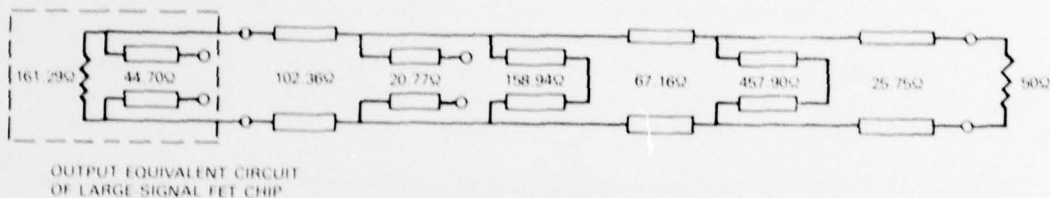
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OUTPUT EQUIVALENT CIRCUIT
OF LARGE SIGNAL FET CHIP

Fig. A6 — Synthesized output matching network for a large-signal, 6- to 18-GHz amplifier using a single-cell, 300-μm (ℓ_w) $\times$ 0.8-μm (ℓ_g) FET
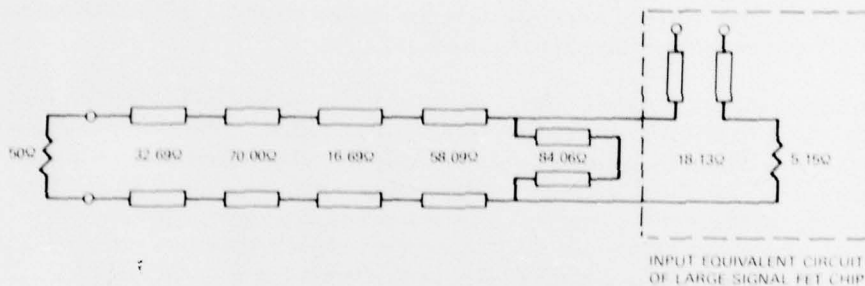
INPUT EQUIVALENT CIRCUIT
OF LARGE SIGNAL FET CHIP

Fig. A7 — Synthesized input matching network for large-signal, 6- to 18-GHz amplifier using a single-cell, 300-μm (ℓ_w) $\times$ 0.8-μm (ℓ_g) FET

Output Matching Network
Slope = 0 dB/oct
Gain = −0.5 dB
ε = 0.144 dB

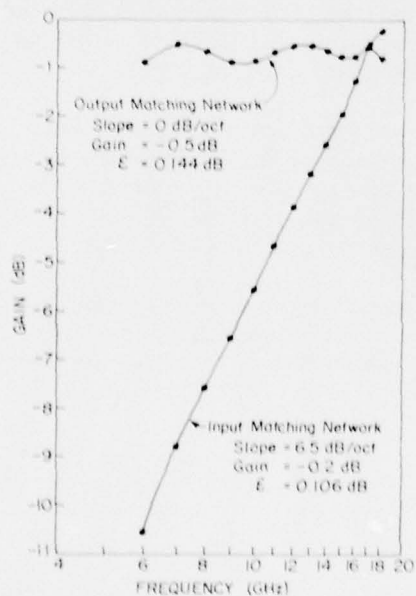Input Matching Network
Slope = 6.5 dB/oct
Gain = −0.2 dB
ε = 0.106 dB

Fig. A8 — Large-signal matching networks with equiripple response characteristics for a single-cell GaAs MESFET. Cell size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g).

GaAs FET
CHIP

INPUT MATCHING
NETWORK

OUTPUT MATCHING
NETWORK

$Z_{01} = 33.8\,\Omega$

$Z_{02} = 67.9\,\Omega$

$Z_{03} = 17.6\,\Omega$

$Z_{04} = 66.7\,\Omega$

$Z_{05} = 96.1\,\Omega$

$Z_{06} = 99.2\,\Omega$

$Z_{07} = 21.8\,\Omega$

$Z_{08} = 158.0\,\Omega$

$Z_{09} = 67.7\,\Omega$

$Z_{10} = 30.6\,\Omega$

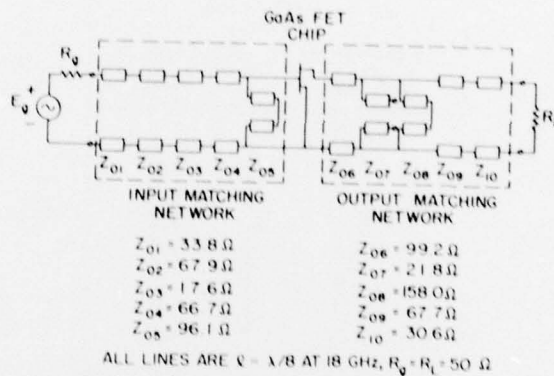ALL LINES ARE $\varrho \sim \lambda/8$ AT 18 GHz, $R_g = R_L = 50\,\Omega$
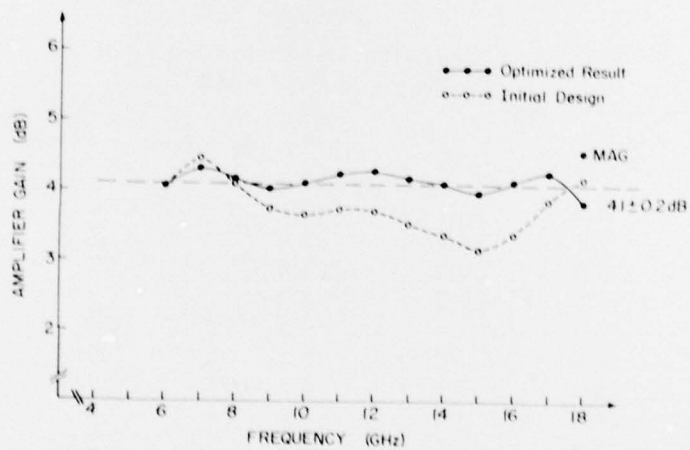
Fig. A9 — Large-signal 6- to 18-GHz
GaAs FET amplifier

Fig. A10 — Calculated Texas Instruments, Inc. GaAs MESFET
large-signal amplifier response

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Table A3 —
Initial Amplifier Gain
Response (Single Cell,
Large Signal)

Frequency (GHz)	Gain (dB)
6.0	4.1
7.0	4.4
8.0	4.0
9.0	3.6
10.0	3.6
11.0	3.7
12.0	3.8
13.0	3.6
14.0	3.5
15.0	3.2
16.0	3.4
17.0	3.9
18.0	4.2

Table A4 — Optimized Amplifier Gain Response
(Single Cell, Large Signal)

Frequency (GHz)	Gain (dB)	Input VSWR	Output VSWR
6.0	4.1	39.9	2.8
7.0	4.3	25.1	2.7
8.0	4.2	18.3	2.7
9.0	4.0	13.7	2.7
10.0	4.1	10.6	2.6
11.0	4.2	8.2	2.5
12.0	4.3	6.5	2.3
13.0	4.2	5.1	2.3
14.0	4.1	4.2	2.3
15.0	4.0	3.4	2.2
16.0	4.1	2.6	2.1
17.0	4.3	2.0	1.6
18.0	3.8	2.0	1.5

Appendix B

PERFORMANCE PROJECTIONS OF HIGH-POWER GaAs MESFETS

In this Appendix, the performance projections of high-power GaAs MESFET's for octave and multioctave amplifiers in the 2- to 18-GHz frequency range are presented. For the single-cell 0.8-μm × 300-μm MESFET chips, the distributed equivalent circuit and the projected optimum gain — bandwidth limitations for the 2- to 18- GHz and 2- to 12-GHz bands are presented in Figs. B1 and B2 and Tables B1 and B2. A single-ended, 2- to 18-GHz-band amplifier can be designed with appropriate gain slopes as predicted by the optimum gain — bandwidth limitations. The corresponding results for the dual-cell device are presented in Figs. B3 and B4 and Tables B3 and B4. Only single-ended amplifier configurations covering the 2- to 18-GHz band are feasible at present because of the practical difficulties in realizing microstrip hybrids to cover this entire frequency band. Note that the impedance matching of the equivalent input resistances R_i (5.57 Ω for the single-cell and 4.09 Ω for the dual-cell case) to 50 Ω across the 2- to 18-GHz band may also impose some problems in the practical realization of the matching network elements.

The distributed equivalent circuit of Texas Instruments, Inc. high-power 1-μm × 1200-μm FETs is presented in Fig. B5. Based on these results, an amplifier covering 4 to 12 GHz has been designed using measured small-signal scattering parameters. The amplifier is shown in Fig. B6 and the computed gain response is presented in Fig. B7. A similar design was established for the 5- to 10-GHz band using the 1200-μm device. The computed gain response for this amplifier is shown in Fig. B8.
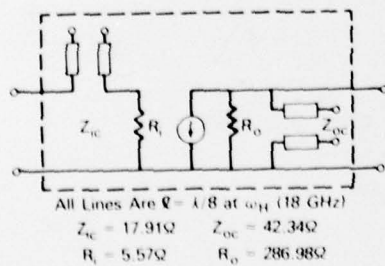

Fig. B1 — Distributed equivalent circuit of a single-cell GaAs MESFET (2-18 GHz). Device: Texas Instruments, Inc, single-cell FET. Cell size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g).

All Lines Are $\ell = \lambda/8$ at ω_H (18 GHz)

$Z_{sc} = 17.91\Omega$ $Z_{oc} = 42.34\Omega$
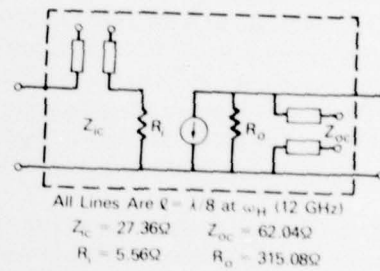
$R_i = 5.57\Omega$ $R_o = 286.98\Omega$

Table B1 — Optimum Gain — Bandwidth Limitations of a Single-Cell GaAs MESFET. Device: Texas Instruments, Inc. Single-Cell FET (2-18 GHz). Cell Size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g).

Gain Slope (dB/oct)	Input Limitation (dB)	Output Limitation (dB)
0 (Flat)	Gain Red. = −7.68	Gain Red. = −1.95
3	Gain Red. = −2.42	Gain Red. = −0.34
6	Gain Red. = 0	Gain Red. = 0

Fig. B2 — Distributed equivalent circuit of
a single-cell GaAs MESFET (2-12 GHz).
Device: Texas Instruments, Inc. single-cell
FET. Cell size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g).

All Lines Are $\ell = \lambda/8$ at ω_H (12 GHz)

$Z_{ic} = 27.36\Omega$ $Z_{oc} = 62.04\Omega$

$R_i = 5.56\Omega$ $R_o = 315.08\Omega$

Table B2 — Optimum Gain — Bandwidth Limitations of a Single-Cell
GaAs MESFET. Device: Texas Instruments, Inc. Single-Cell FET (2-12 GHz)
Cell Size: 300 μm (ℓ_w) × 0.8 μm (ℓ_g).

Gain Slope (dB/oct)	Input Limitation (dB)	Output Limitation (dB)
0 (Flat)	Gain Red. = −7.55	Gain Red. = −1.20
3	Gain Red. = −3.35	Gain Red. = 0
6	Gain Red. = 0	Gain Red. = 0

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All Lines Are ℓ = λ/8 at ω_H (18 GHz)

$Z_{ic} = 9.37Ω$ $Z_{oc} = 24.84Ω$
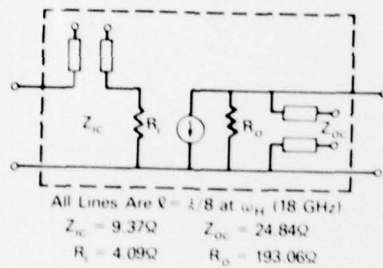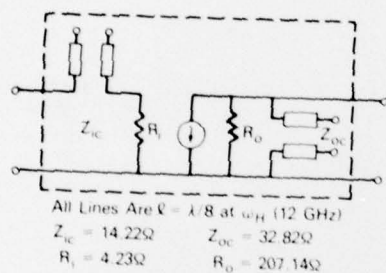
$R_i = 4.09Ω$ $R_o = 193.06Ω$

Fig. B3 — Distributed equivalent circuit of a dual-cell GaAs MESFET (2-18 GHz). Device: Texas Instruments, Inc. dual-cell FET. Cell size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g).

Table B3 — Optimum Gain — Bandwidth Limitations of a Dual-Cell GaAs MESFET. Device: Texas Instruments, Inc. Dual-Cell FET (2-18 GHz). Cell-Size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g).

Gain Slope (dB/oct)	Input Limitation (dB)	Output Limitation (dB)
0 (Flat)	Gain Red. = −6.36	Gain Red. = −2.31
3	Gain Red. = −1.24	Gain Red. = −0.60
6	Gain Red. = 0	Gain Red. = 0

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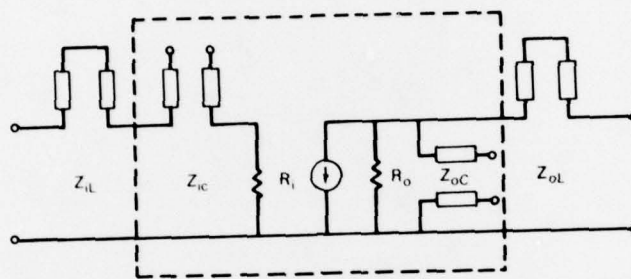
Fig. B4 — Distributed equivalent circuit of a dual-cell GaAs MESFET (2-12 GHz). Device: Texas Instruments, Inc. dual-cell FET. Cell size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g).

All Lines Are $\ell = \lambda/8$ at ω_H (12 GHz)

$Z_{ic} = 14.22\Omega$ $Z_{oc} = 32.82\Omega$

$R_i = 4.23\Omega$ $R_o = 207.14\Omega$

Table B4 — Optimum Gain — Bandwidth Limitations of a Dual-Cell GaAs MESFET. Device: Texas Instruments, Inc. Dual-Cell FET (2-12 GHz). Cell Size: 300 μm (ℓ_w) $\times$ 0.8 μm (ℓ_g).

Gain Slope (dB/oct)	Input Limitation (dB)	Output Limitation (dB)
0 (Flat)	Gain Red. = -6.08	Gain Red. = -1.40
3	Gain Red. = -1.97	Gain Red. = -0.06
6	Gain Red. = $\quad$ 0	Gain Red. = $\quad$ 0

Fig. B5 — Distributed equivalent circuit of a high-power GaAs MESFET. Device: Texas Instruments, Inc. GaAs MESFET. Cell size: 1200 μm (ℓ_w) $\times$ 1 μm (ℓ_g).
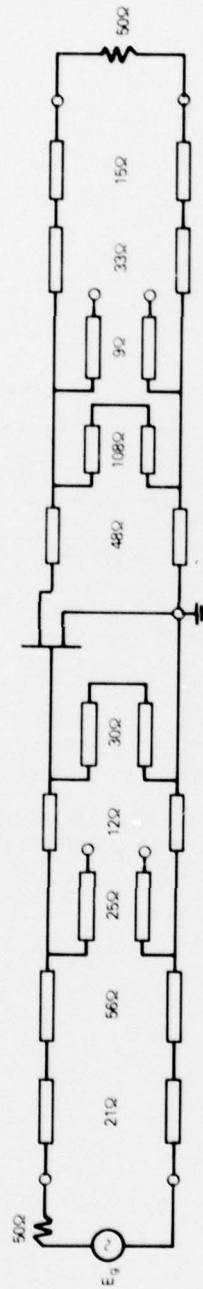
All Lines Are $\ell = \lambda/8$ at 12 GHz

(a) 4-12 GHz

$Z_{iL} = 22.56\Omega$ $Z_{oL} = 7.74\Omega$

$Z_{iC} = 8.05\Omega$ $Z_{oC} = 29.70\Omega$

$R_i = 7.8\Omega$ $R_o = 121.33\Omega$

(b) 2-12 GHz

$Z_{iL} = 23.42\Omega$ $Z_{oL} = 8.81\Omega$

$Z_{iC} = 8.71\Omega$ $Z_{oC} = 29.32\Omega$

$R_i = 7.75\Omega$ $R_o = 129.68\Omega$

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Fig. B6 — A 4- to 12-GHZ GaAs MESFET amplifier. Device: Texas Instruments, Inc. GaAs MESFET. Cell size: $1200~\mu m~(\ell_w) \times 1~\mu m~(\ell_g)$.
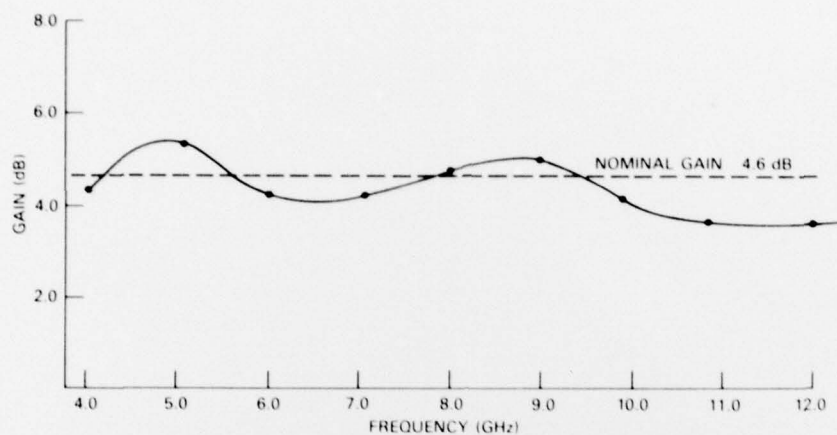
Fig. B7 — Computed 4- to 12-GHz GaAs MESFET amplifier response. Device: Texas Instruments, Inc. GaAs MESFET. Cell Size: 1200 μm $(\ell_w) \times 1 \mu m$ (ℓ_g). Bias: 6.0 VDC (V_{DS}), -2.0 VDC (V_{GS}).
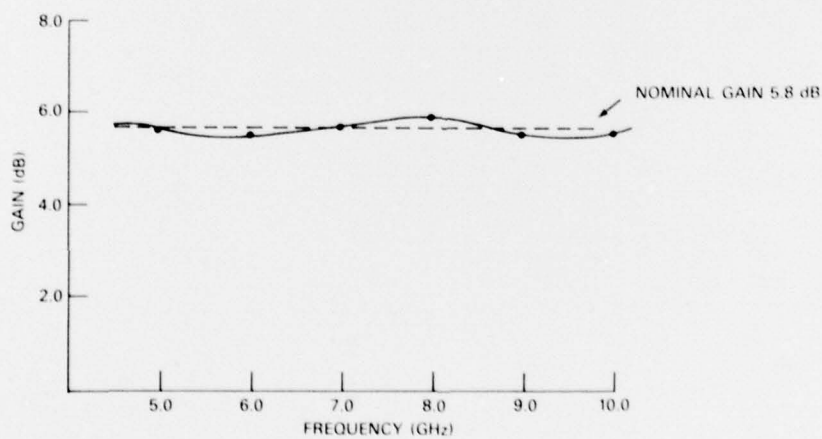

Fig. B8 — Computed 5- to 10-GHz GaAs MESFET amplifier response. Device: Texas Instruments, Inc. GaAs MESFET. Cell size: 1200 μm $(\ell_w) \times 1 \mu m$ (ℓ_g). Bias: 6.0 VDC (V_{DS}), -2.0 VDC (V_{GS}).

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